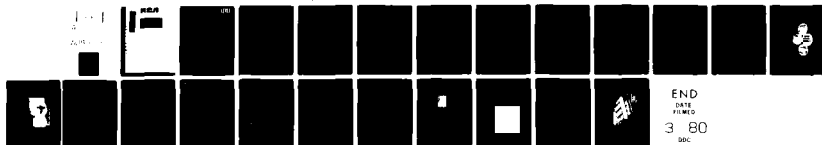


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FINAL REPORT

LOW COST, LOW POWER DISSIPATION
MICRO-SIGNAL PROCESSOR FOR
ACOUSTIC SIGNAL PROCESSING (U)

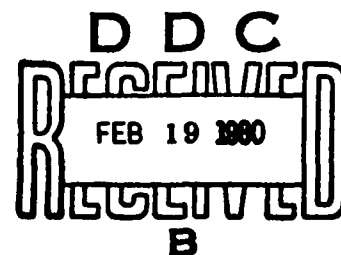
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20. ABSTRACT (cont.)

All necessary functions for a self-contained, stand alone acoustic processor were incorporated in a 410 cu. cm. feasibility brass-board, dissipating an average of 50 mw. All essential components were either CMOS or CMOS/SOS, including the standard commercially available 1802 microprocessor, and, a special LSI multiplier required for expediting the computations needed for the FFT. Major hardware and software issues are discussed, followed by an exposition of emerging technology IC's, leading to even smaller, lower cost, lower power dissipation processors. In particular, new compatible monolithic filtering will improve performance by converting the analog conditioning requirements to a single chip design, which can be combined with five other existing chips for a complete acoustic processor.

The development of an acoustic signal processor utilizing monolithic filtering is continuing under ONR Contract No. N00014-79-C-0566.

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LOW COST, LOW POWER DISSIPATION
MICRO-SIGNAL PROCESSOR
ACOUSTIC SIGNAL PROCESSING (U)

ABSTRACT

A low cost, low power dissipation micro-signal processor has been designed and built for application to deployed sensors. Using latest technology, state-of-the-art components, this microprocessor based system has been programmed, and demonstrated in performing 1024 point fast Fourier transforms (FFT's) on 8-bit input data within one second, as well as a variety of associated data acquisition and control functions.

All necessary functions for a self-contained, stand alone acoustic processor were incorporated in a 410 cu. cm. feasibility brassboard, dissipating an average of 50 mw. All essential components were either CMOS or CMOS/SOS, including the standard commercially available 1802 microprocessor, and a special LSI multiplier required for expediting the computations needed for the FFT. Major hardware and software issues are discussed, followed by an exposition of emerging technology processors. In particular, new compatible monolithic filtering will improve performance by converting the analog conditioning requirements to a single chip design, which can be combined with five other existing chips for a complete acoustic processor.

DESCRIPTION OF MICRO-SIGNAL PROCESSOR

A functional block diagram of the acoustic micro-signal processor is shown in Figure 1. Although consisting basically of a digital microprocessor system, the processor contains a significant amount of analog circuitry, and, as will be shown later can benefit from even more analog pre-processing or conditioning. Each of the major functions will be described.

Micro-Signal Processor Functional Block Diagram

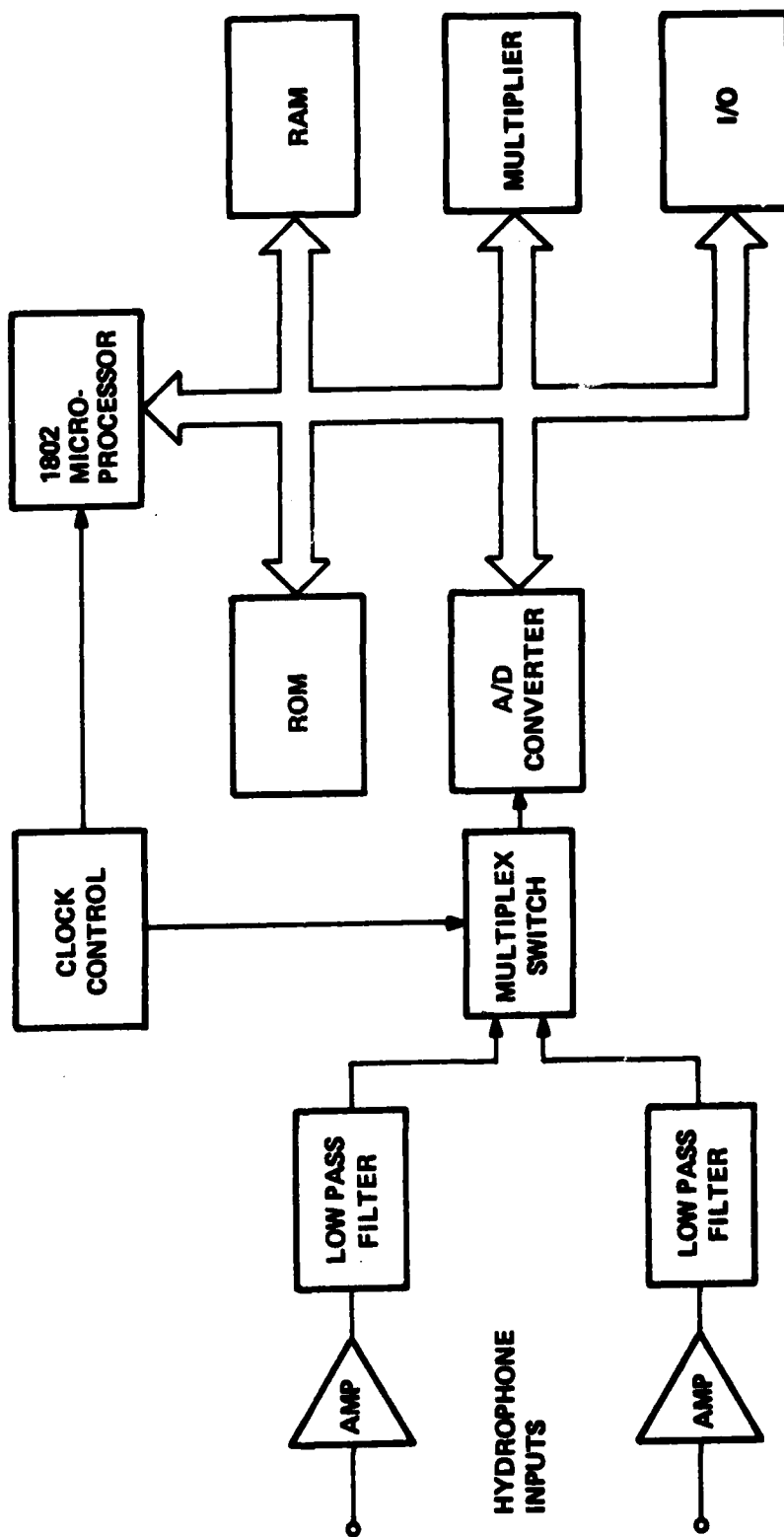


FIG. 1

Analog Conditioning

First, an AGC amplifier is required to provide for signals with dynamic ranges greater than what our 8-bit low power monolithic A/D converter can accommodate, since we are frequently dealing with dynamic ranges of 100 db or more. Next, we need low pass filters for pre-sampling to prevent aliasing. Sharp cutoffs, requiring six poles or more are generally necessary to minimize sampling rates.

In addition, bandpass filters are advantageous. They can be used for activity detection, i.e., for monitoring energy in given bands to control turn-on of the higher power consuming microprocessor circuitry prior to attempting target classification. Also, they can be used to provide for, or improve the spectral resolution which the microprocessor is capable of providing. That is, even though we can now perform relatively sophisticated digital processing such as the fast Fourier transform, it will be more effective (lower power, higher throughputs) to off-load the micro using new monolithic filter techniques.

Following any filtering functions, the remainder of the analog conditioning consists of multiplexing multi-channel inputs and analog to digital conversion.

All of these functions must of course be accomplished with the low cost, low power consumption circuitry consistent with the rest of the processor. The key to doing this has recently been demonstrated and is being applied to acoustic signal processing, i.e., switched capacitor monolithic filters. This will be described after discussing the performance of the micro-signal processor.

Multiplier

This, and the remaining signal processing functions are all digital in nature. Because of the need for the relatively high speed computations - particularly the FFT - a hardware multiplier is required to augment the microprocessor. Software multiplication would be much too slow and/or power consuming. Two types of CMOS/SOS, LSI multipliers have been built at RCA, useful for this application. One is an 8x8 bit parallel chip -used in the brassboard of the acoustic processor shown in Figure 2, and the other (more recent circuit) is an 8 or 16-bit* serial-parallel chip designed specifically for the standard microprocessor interface, and, includes an accumulate function as well. The latter circuit is better suited for the processor and will be incorporated in subsequent versions.

Microprocessor

While our original micro-signal processors were based on the commonly available, low power CMOS, 1802 microprocessor, new technology CMOS/SOS, commercial micros are becoming available during the latter part of 1979 which can improve the performance of the acoustic processor. One is the 1804 which is software compatible with the 1802, but will provide twice the speed at about the same level of power dissipation. Also, it will contain 2k bytes of ROM and 64 bytes of RAM, to reduce outboard memory requirements. The second new part which can beneficially impact our acoustic processors is the CMOS/SOS 8085; compatible with the present NMOS versions, significantly more throughput will be possible compared to the present configuration.

Although all of these micros are 8-bits wide, and most of our computations are done in 8-bit precision, double precision has been used, when necessary.

*While we have been successfully able to perform all necessary computations up to now with 8-bit precision, the 16-bit feature will be useful for some of the higher resolution and more demanding requirements.

Memory

Most of the micro-signal processor's memory is ROM. This contains all instructions, constants and coefficients. For one of the applications in acoustic signal processing, to be elaborated upon in the next section, the total ROM requirements could be contained within a 4k byte capacity - with some spare capacity for expansion or program modification. We consider two types of ROM for our processors; mask programmable and electronically programmable (alterable). In either case, we must use CMOS or MOS SOS technology. The former type is lower cost in production but requires new part types for changes or retrofit, while the latter type provides the flexibility for modification in a variety of situations. For example, one could, by an external connector and an input device, re-program the acoustic processor prior to deployment to meet any one of a number of mission requirements. The EPROM's are now becoming available in the low power dissipation technology and their application must be considered, trading-off flexibility and cost for given production runs.

The RAM used for data collection and intermediate result storage and manipulation was 3k bytes in our initial model, and can readily be expanded or cut in size to meet specific applications.

FEASIBILITY BRASSBOARD MODEL

Figures 2 and 3 show the initial low cost, low power dissipation feasibility brassboard, built to demonstrate acoustic signal processing capability. The brassboard was configured on 11.4 cm diameter boards, consistent with a standard "A" size buoy canister, as shown in Figure 3.

Modules For Brassboard of Acoustic Micro-Signal Processor

FIG. 2

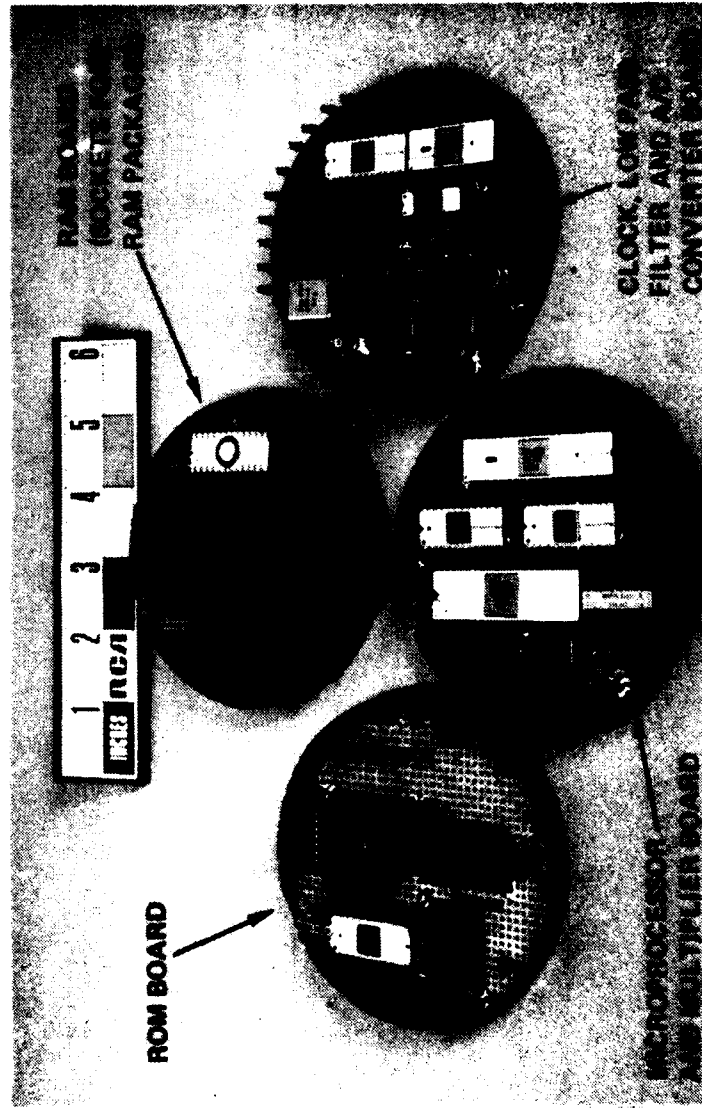


FIG. 3 **Assembly of Brassboard Modules For Test**



The ROM board in this model was populated with ultra-violet erasable 2k x 8 bit NMOS parts, for experimentation purposes. The sockets on the RAM board will accept commercially available CMOS or CMOS/SOS 4k x 1 bit parts. The A/D converter and multiplier are CMOS/SOS devices, developed at RCA. The microprocessor and miscellaneous control logic circuits are CMOS. The analog conditioning circuits - amplifier, active filter -use low power dissipation IC operational amplifiers with discrete components. (It will be shown how to simplify these latter functions with the monolithic switched-capacitor filter array in the next section.)

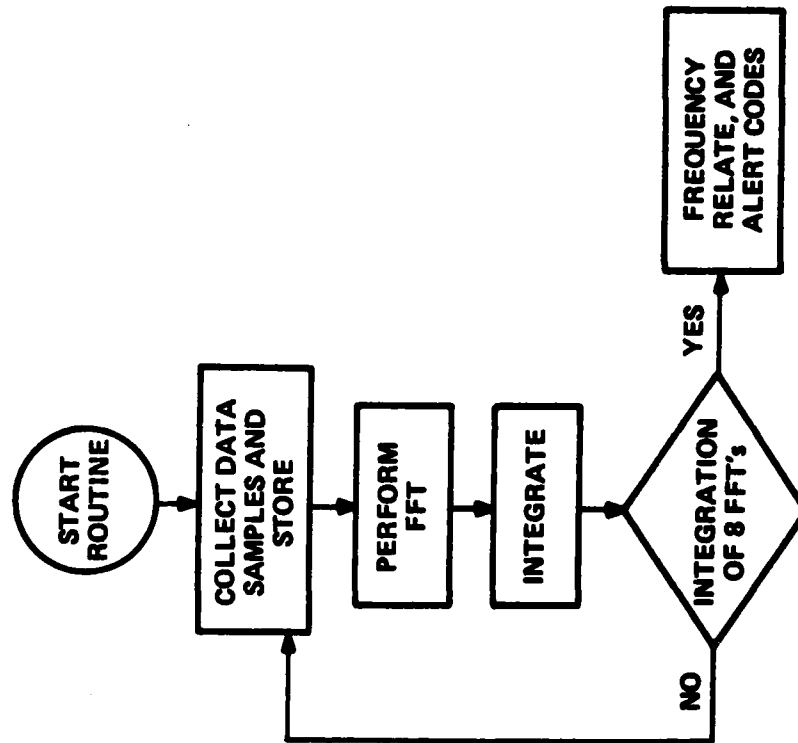
This model was designed for a single channel hydrophone input and the A/D conversion rate is 820 Hz. The microprocessor's system clock is generated by a 2.516 MHz crystal. The unit was programmed to perform spectral analysis using a 1024 point fast Fourier transform (FFT), followed by integration and some line relationship analysis. The overall flow diagram showing the major sub-routines, and the appropriate time for their performance is shown in Figure 4.

The FFT was performed with 8-bit precision, using conditional scaling between (butterfly) passes to maintain maximum accuracy. The memory allocation for the crossboard, Figure 5 gives the breakdown of the individual function requirements. Figure 6 is a typical plot showing the integrated FFT output results from an analog magnetic tape recording.

The essential components of this acoustic processor, when populated with the final configuration CMOS ROM, dissipate about 50 mw, operating continuously. The total volume occupied in this experimental version is 410 cu. cm. It will be shown how the parts count (and hence, cost and size) as well as power dissipation can be reduced with the new emerging technology.

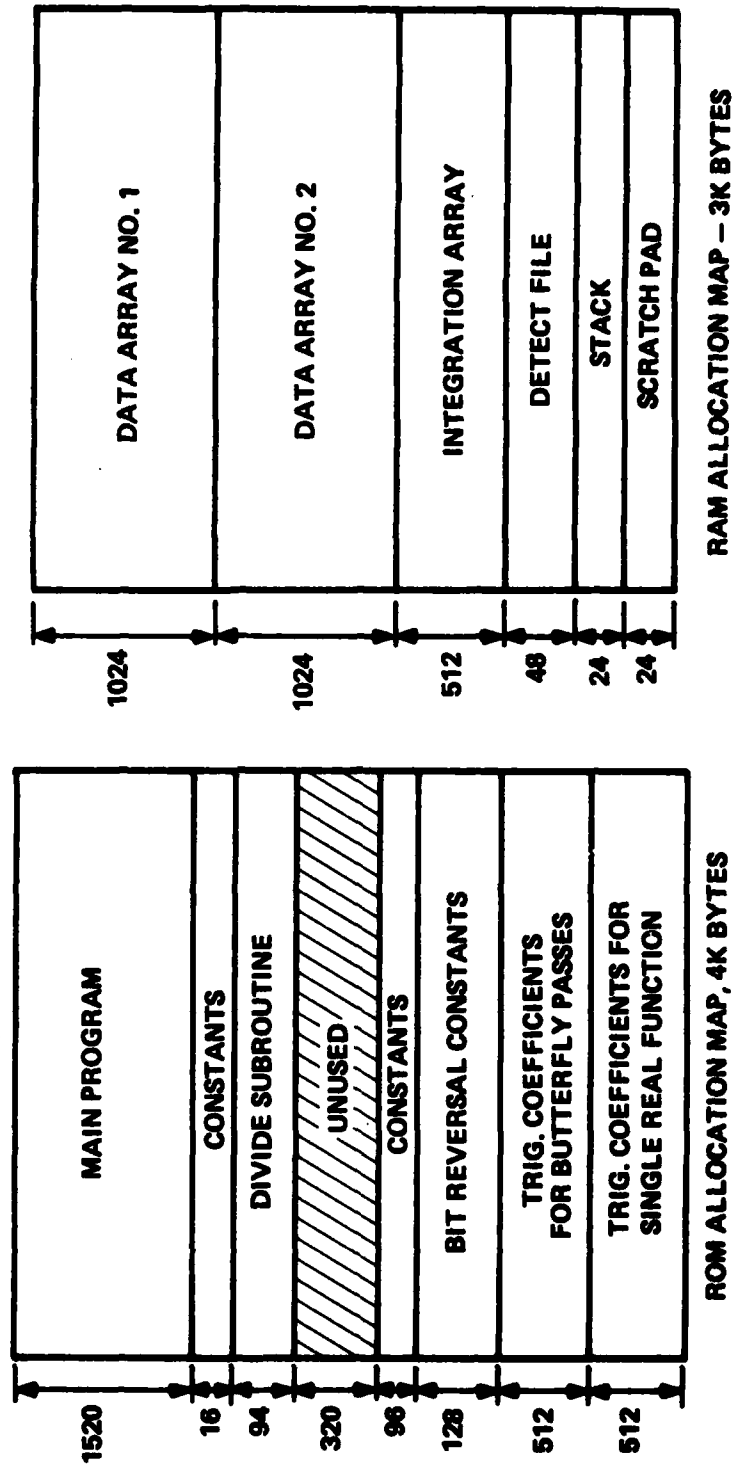
FIG. 4

Processor Functions



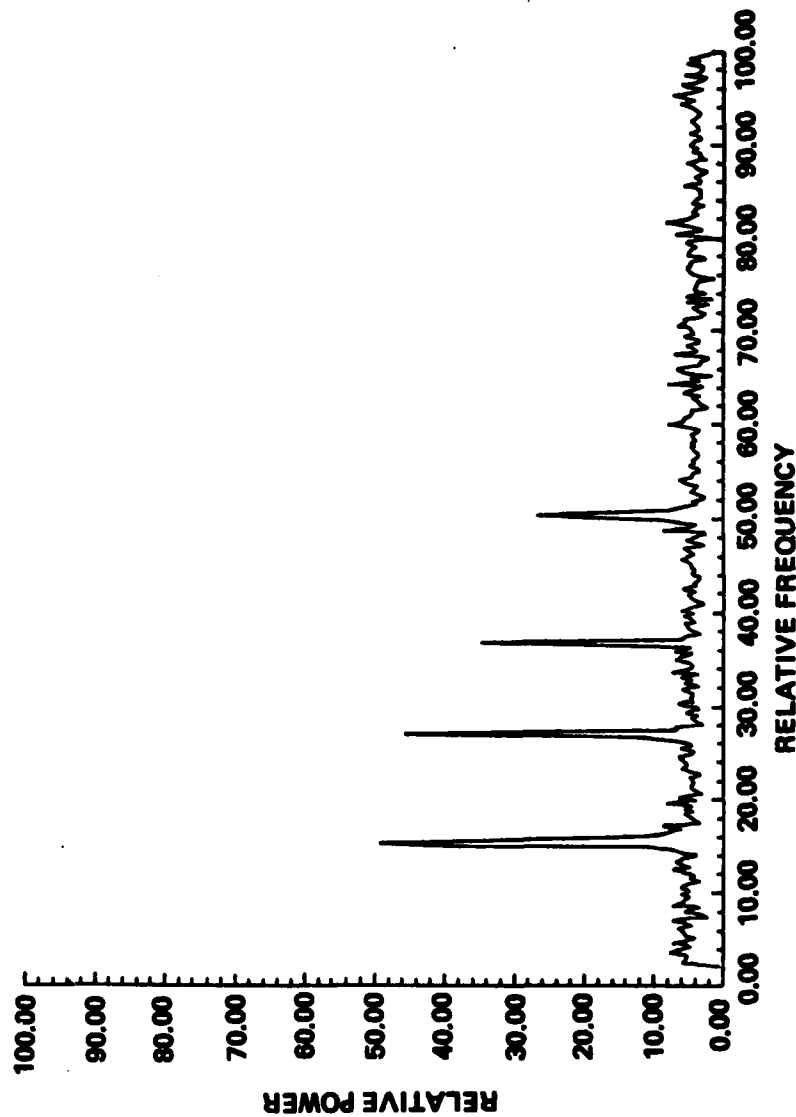
Memory Requirements

FIG. 5



Output From Acoustic Signal Processor After Performing 1024 Point FFT's and Integrating 8 Times

FIG. 6



Other Applications

The acoustic processor assembly described contains beginning-to-end logic and storage capability to perform a variety of other functions besides spectral analysis. For example, one could perform beamforming with the same basic complement. In one approach, (when the microprocessor is upgraded to the 1804 and a multi-channel front-end is added), time domain beamforming can be accomplished with up to 16 element hydrophone arrays, computing 12 beams, at an input sampling rate of 800 Hz. Alternatively, larger arrays with fewer beams and/or lower bandwidths can be accommodated with the single microprocessor.

Also, cross-correlation can be performed as an alternative to the FFT for spectral analysis. For example, by cross-correlating the input signal with a sequence of periodic pulses it is possible to detect the presence of a given frequency buried in noise. This amounts to sampling, storing and accumulating (or adding). This technique obviates the need for the multiplier chip but this savings must be traded-off against the storage capacity required and time required to search for all frequencies of interest.

Finally, the acoustic processor possesses the intelligence for sophisticated communications transmission and reception. The microsignal processor can be programmed for use in low probability of intercept (LPI) modulation systems where multi-tone coding is used to format messages. Using 64-tone frequency shift keying (FSK), where each tone or symbol conveys 6 bits of information, bit error rates and/or radiated power levels can be reduced compared to that of standard digital communication links.

SWITCHED CAPACITOR MONOLITHIC FILTERS

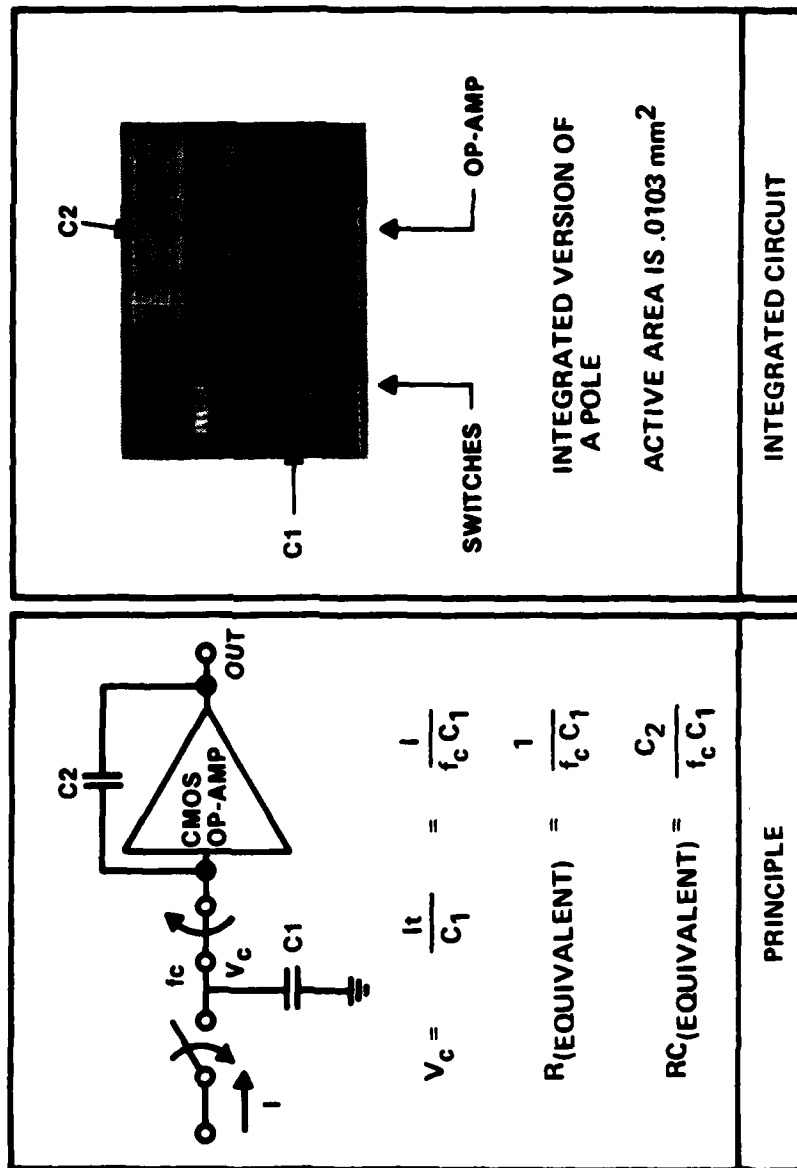
In order to provide for even greater spectral resolution than what the digital micro-signal processor can perform in real-time, while simultaneously reducing the complexity and power dissipation of the required gain and pre-sampling filter circuits a new technique for monolithic integration of analog functions has been developed.

The key to low power dissipation monolithic analog conditioning is the use of CMOS operational amplifiers (which have already been proven in A/D converter designs as well as other linear IC's), and, switched capacitor techniques, to simulate accurate resistors. The principle is shown in Figure 7. By switching the current in and out of the input capacitor, C1, of an op-amp with feedback capacitor, C2, it is seen that an RC equivalent, or "pole", is achieved which depends solely on a capacitor ratio (the precision of which is easy to achieve in MOS technology, with temperature tracking) and the switching frequency.

Not only can we then build well defined poles, which are the building blocks of filters, but we can move them, if desired, under clock control, from a crystal source and divider chain.

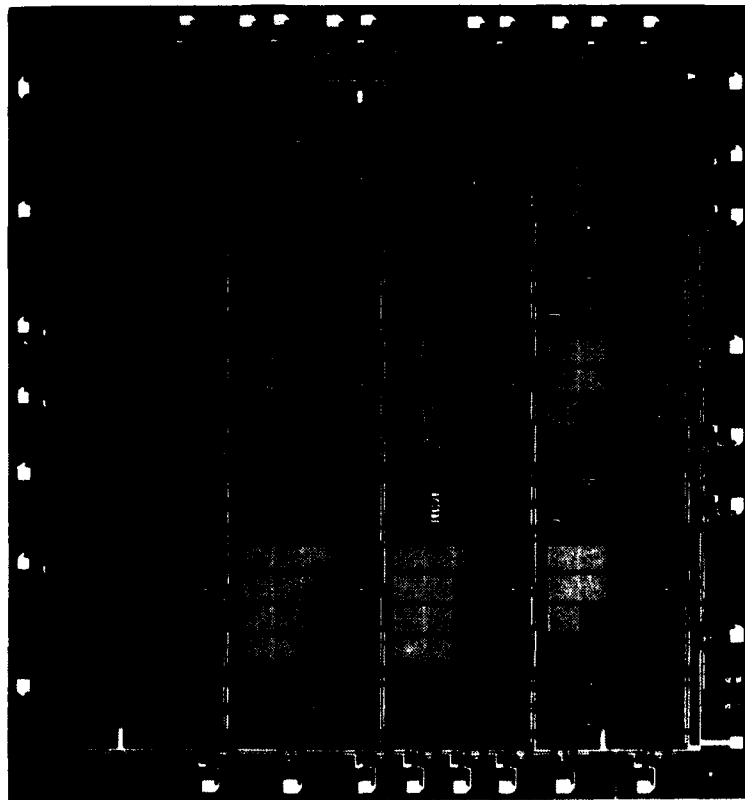
An LSI array of such cells has been built for demonstration, and test. Figure 8 is the microphoto of a chip containing 12 poles and two programmable amplifiers which were connected to meet typical analog conditioning requirements for a smart sensor. The different input capacitor areas are noted, for different filter responses. The poles were interconnected to provide a sharp cutoff 6-pole low pass

FIG. 7 **Switched Capacitor Filter/Amplifier Array**



LSI Filter/Amplifier Chip For "Analog Conditioning" For Smart Sensors

FIG. 8



- 12 POLES FOR LOW PASS AND BANDPASS FILTERS
- 42 dB PROGRAMMABLE GAIN
- 1 mW DISSIPATION

filter for pre-sampling, 2, 2-pole low pass filter for a feature extraction purposes. The uncommitted amplifiers on the right side of the chip are programmable in 6 db steps and can provide up to 42 db of gain. The entire circuit dissipates 1 mw and has been tested, with excellent results of temperatures form -25°C to 80°C .

It is planned to customize this array, for acoustic signal processing, for use in conjunction with the existing brassboard model. This will then reduce the complexity and power while simultaneously providing improved performance.

CONCLUSIONS

Using the technology just described, and, existing or developmental IC's, an assembly of 6 chips, placed in leadless hermetic packages on a ceramic carrier, will provide all of the functions required for a versatile acoustic processor. The 6 chips shown in Figure 9 are 1) analog conditioner and filter bank, 2) A/D converter, 3) microprocessor, 4) multiplier, 5) ROM and 6) RAM. This 5 cm x 2.5 package can meet the most demanding size constraints and can be built with state-of-the-art parts.

Such assemblies can substantially improve expendable, battery operated acoustic signal processing systems by virtue of their low cost and low power dissipation. Possessing a relatively high degree of sophisticated signal processing capability they can aid in problems requiring high spectral analysis and target classification and can be considered in distributed form for more demanding applications.

**Chip-Carrier Package Assembly (5x2.5 cm)
For Acoustic Micro-Signal Processor**

FIG. 9

